Phillips Scientific

16 Channel Individual Start-Stop TDC

CAMAC MODEL 7187 7187H

FEATURES

* Model 7187 Features NIM Inputs with LEMO Connectors
* Model 7187H Features Differential ECL with Header Connector
* Individual START and STOP Inputs for Each Channel
* Less Than 7.2 µSec Conversion and Processing Time
* 12-Bit Dynamic Range, Resolution to 25 pSec/Count
* Programmable Pedestal Correction
* Sparse Data Scan with Lower and Upper Time Cuts
* Fast CLEAR and GATE Window
* Built-in Test Feature Checks TAC and Digitization Sections

DESCRIPTION

The Model 7187/H TDC implements 16 channels of Time to Amplitude Conversion (TAC), each with its own START and STOP, followed by a digital processing section and CAMAC interface in a double width CAMAC module. To minimize data readout time, the module performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following release of the GATE input. It may be delayed by a user-programmable amount to allow time for derivation of fast CLEAR signals.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel fast CLEAR or CAMAC Clear commands.

Four user selectable time ranges are provided in a given configuration:

Standard Configuration	
Range	Resolution
100 nSec	25 pSec
200 nSec	50 pSec
400 nSec	100 pSec
800 nSec	200 pSec

Alternate Configuration	
Range	Resolution
1 µSec	.25 nSec
2 µSec	.50 nSec
4 µSec	1.0 nSec
8 µSec	2.0 nSec

Note: All channels need not have the same scale factors. Custom ranges are available when ordering.

INDIVIDUAL START and STOP INPUTS

**7187** : Fast negative NIM, direct coupled input (50 ohm impedance); minimum pulse width 10nSec.

7187H : 100 ohm, differential ECL, 100mV threshold. Minimum input pulse width 10nSec.

In case of multiple signals within a single gate, only the first one will be recognized.

GATE, CLEAR, TEST START and TEST STOP INPUTS

7187 : Two bridged LEMO inputs to facilitate daisy chaining (5.1K ohm impedance). Terminate at end of chain with 50 ohms.

7187H : Two pairs of differential ECL inputs to facilitate daisy chaining. Terminate at end of chain with 110 ohms.
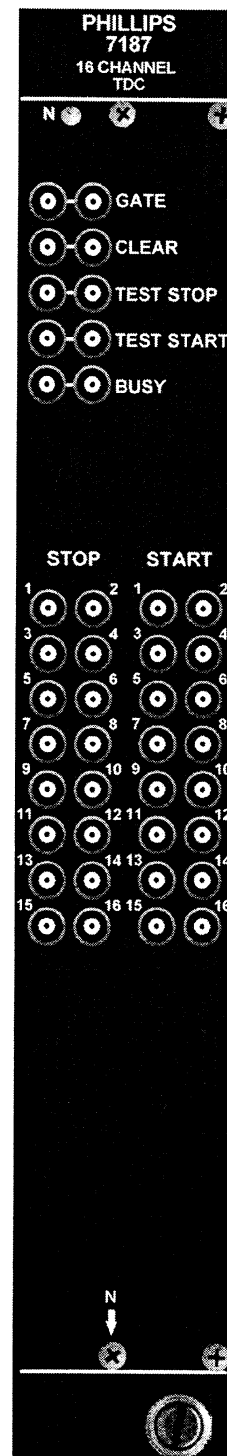
Conversion Time	:	7.2µSec maximum. Digitization begins 750nSec after the trailing edge of GATE to allow time for settling and for accepting CLEAR signals. Digitization may be delayed by 0 to 16µSec in 62.5nSec increments with external jumpers. The increased delay may be used to allow a greater acceptance window for CLEAR signals. For ranges less than 800 nSec full scale, increasing the delay such that digitization begins more than 4µSec after the first STOP signal may result in a degradation in module performance.
GATE Input	:	When active, enables START and STOP inputs. Conversion starts as soon as it is released. Assert time: Must be asserted at least 15nSec before the earliest START. Release time: Must be released no earlier than the last STOP.
CLEAR Input	:	Resets the Hit Register and the front ends as follows: **100, 200, 400, 800nSec Ranges:** **t < (trailing edge of GATE - 850nSec):** Resets any channels that have received START signals; no effect on digitization. **(trailing edge of GATE - 700nSec) < t < Start of Digitization** : Resets front ends and aborts digitization cycle. **t > Start of Digitization** : Resets front ends; no effect on digitization. **1, 2, 4, 8µSec Ranges:** **t < (trailing edge of GATE - 2.2µSec)** : Resets any channels that have received START signals; no effect on digitization. **(trailing edge of GATE - 1.9µSec) < t < Start of Digitization** : Resets front ends and aborts digitization cycle. **t > Start of Digitization** : Resets front ends; no effect on digitization. BUSY is asserted following CLEAR to allow time for the front ends to fully reset.
TEST START/STOP	:	Used in conjunction with GATE to apply a test START/STOP interval to all channels.

BUSY Output

LEMO (7187)	:	LEMO output connector. NIM current switching bridged output (32 mA).
ECL (7187H)	:	Differential ECL output; Two pairs double row pins. Active as follows:

- From the trailing edge of GATE until the event has been aborted by CLEAR or has been fully digitized and read out through the sparse data port. BUSY follows the Hit Register and thus may also be released by clearing the Hit Register.
- For 800 nSec following CLEAR (2.4µSec for ranges 1µSec).
- During any CAMAC addressing of the module.

FRONT END PERFORMANCE

A dithered mode may be selected by the user for improved performance in spectroscopy analysis. It should be disabled when working within the bottom or top 1.5% of the module's range or for those measurements not creating histograms of data.

Linearity	:	Integral : Less than 4 counts over 10% to 90% of range. Differential : Less than 0.025% of full scale maximum. 　　　　Non-Dithered : ±0.5 bins typically 　　　　Dithered : ±0.1 bins typically

FRONT END PERFORMANCE *(continued)*

Noise, Jitter : *Typically 20pSec RMS.*

Crosstalk : *Less than 3 LSB between adjacent channels.*

START/STOP : *20nSec internal offset; Front ends are offset by this amount for improved linearity*
Pedestal *and to allow use of full dynamic range.*

Stability : *Gain : 100 ppm/ °C typically.*
Offset : 0.15 counts/ °C typically.

Power Supply Requirements : *+ 6V @ 2.8 Amps typically*
– 6V @ 3 Amps typically
+24V @ 180 mA typically
Forced air cooling is recommended.

ADDITIONAL TEST FEATURES

Calibration : *Simulates a GATE/START/STOP sequence under CAMAC control to verify*
Check *operation of the module. CAMAC selectable nominal 1/3 or 2/3 full scale calibration for each full scale range. Not intended for use in calibrating the module.*

CAMAC : *Loads a predetermined pattern to simulate the outputs of the A/D converters.*
Check *Useful for verifying the operation of the digital processing sections of the module.*

SPARSIFICATION and LAM OPERATION

Separate pedestals and upper and lower thresholds may be set for each channel. They are enabled using bits in the Control Register. Pedestals in signed 2's complement format are added to the data before threshold comparison. Bits in the Hit Register are set during digitization for those channels whose pedestal corrected data falls within their upper and lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data reads present only those channels with bits set in the Hit Register, starting with the highest numbered channel. As channels are read, their Hit Register bits are reset; when the final channel has been read LAM is reset. LAM is also reset when the Hit Register is reset.

DATA WORD FORMAT

16	13	12	1
Channel ID		Channel Data	

CONTROL REGISTER FORMAT

16	9	8 4	3	2	1
Conversion Delay (Read Only)		0	UT Enable	LT Enable	PED Enable

CAMAC DATAWAY OPERATION

F(0)·A(X) : *Read event data memory for Channel (X+1). Data word as described above.*

F(1)·A(X) : *Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).*

F(4)·A(0) : *Read Sparse Data. Only those channels with data that falls between their upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.*

F(6)·A(0) : *Read the Control Register. Format described above.*

CAMAC DATAWAY OPERATIONS *(continued)*

F(6)·A(1) : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.

F(8) : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(9) : Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(10) : Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

F(11)·A(0) : Reset the Control Register. Occurs on S2 strobe.

F(11)·A(1) : Reset the hit register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11)·A(2) : Reset the test register. Occurs on S2 strobe.

F(11)·A(3) : Reset the hit register, LAM and data memory. Occurs on S2 strobe.

F(16)·A(X) : Write to data memory for channel (X+1).

F(17)·A(0) : Select the Pedestal Memory for the next F1 or F20 operation.

F(17)·A(1) : Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)·A(2) : Select the Upper Threshold Memory for the next F1 or F20 operation.

F(17)·A(4) : Select the Test Register for the next F20 operation.

F(19)·A(0) : Set the Control Register bits. Format described above.

F(20)·A(X) : Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is ±4095; threshold ranges are 0 to 4095.

F(20)·A(X) : Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is ±4095; threshold ranges are 0 to 4095.
Program the test register if it was selected by the most recent F17 operation.
A0 : Test pattern = 001001001001
A1 : Test pattern = 010010010010
A2 : Test pattern = 100100100100
A3 : Test pattern = 111111111111

F(23)·A(0) : Reset the Control Register bits. Format described above.

F(24) : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(25)·A(0) : Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.

F(25)·A(1) : Test. Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)·A(2) : Test. Runs a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

F(26) : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

C, Z : Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I : Inhibits TDC Front End.