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Sub-10 nm Monolayer MoS_2 Transistors Using Single-Walled Carbon Nanotubes as an Evaporating Mask

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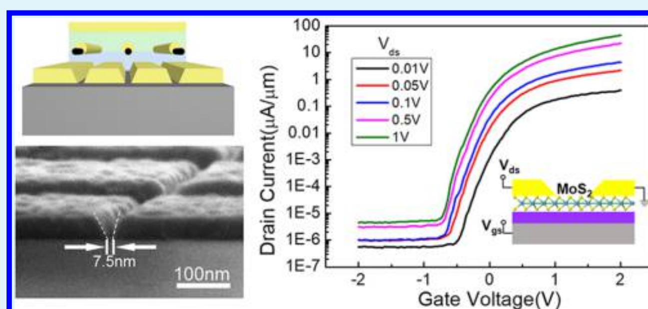
Supporting Information

ABSTRACT: Transition-metal dichalcogenides are promising challengers to conventional semiconductors owing to their remarkable electrical performance and suppression of short-channel effects (SCEs). In particular, monolayer molybdenum disulfide has exhibited superior suppression of SCEs owing to its atomic thickness, high effective carrier mass, and low dielectric constant. However, difficulties still remain in large-scale stable fabrication of nanometer-scale channels. Herein, a method to fabricate electrodes with sub-10 nm gaps was demonstrated using horizontally aligned single-walled carbon nanotubes as an evaporation mask. The widths of the nanogaps exhibit robust stability to various process parameters according to the statistical results. Based on these nanogaps, ultrashort-channel length monolayer MoS_2 field-effect transistors were produced. Monolayer MoS_2 devices with a 7.5 nm channel length and a 10 nm thick HfO_2 dielectric layer exhibited excellent performances with an ON/OFF ratio up to 10^7, a mobility of 17.4 $cm^2/V{\cdot}s$, a subthreshold swing of about 120 mV/dec, and a drain-induced barrier lowering of about 140 mV/V, all of which suggest a superior suppression of SCEs. This work provides a universal and stable method for large-scale fabrication of ultrashort-channel 2D-material transistors.



KEYWORDS: *MoS_2, carbon nanotube, field-effect transistor, sub-10 nm, short-channel effects*

INTRODUCTION

As silicon-based field-effect transistors (FETs) are scaled down into the nanometer regime, short-channel effects (SCEs) have become a significant issue.[1−3] In these short-channel transistors, direct source-to-drain tunneling and loss of gate electrostatic control cause serious degradation of the FET performance.[4] As a consequence, drain-induced barrier lowering (DIBL) and hot carrier injection are induced as two typical SCEs. To suppress these SCEs, channel materials should have a high carrier effective mass, a low in-plane dielectric constant, and a thickness less than one-third of the channel length.[5−8]

Monolayer molybdenum disulfide (MoS_2) is a 2D semiconductor with notable merits such as a large direct band gap of 1.9 eV,[9] a high effective mass of $0.48m_e$ (where m_e is the electron mass),[10] a low in-plane dielectric constant of 3.3,[11] and an atomic-layer thickness of 0.65 nm.[12] Thus, monolayer MoS_2 exhibits superior suppression of SCEs and a suitability for sub-10 nm FETs in particular. However, fabrication of sub-10 nm channel length transistors remains a challenge because of the limits of lithography.[4,13] Several methods have been developed to fabricate sub-10 nm gaps, such as Bi_2O_3 thin-film nanogaps[8] and graphene nanogaps,[14] but these nanogaps form randomly and lead to a low yield of sub-10 nm MoS_2 FETs.

RESULTS AND DISCUSSION

Single-walled carbon nanotubes (SWCNTs) have diameters that are only several nanometers and can been employed as an evaporation mask for the fabrication of nanogaps.[15,16] Carbon nanotube films have been applied in the fabrication of nanostructures in our previous work.[17,18] Here, we demonstrate a process-stable method for the large-scale fabrication of sub-10 nm channel MoS_2 FETs using a horizontally-aligned SWCNT film as an evaporation mask. Benefiting from the uniform and nanometer-scale diameters of the SWCNTs, the nanogap widths are typically less than 10 nm and are stable with varying fabrication process parameters. A fabricated back-gated monolayer MoS_2 FET comprising a 7.5 nm channel length and a 10 nm thick HfO_2 dielectric layer possesses a current ON/OFF ratio up to 10^7, a subthreshold swing of 120 mV/dec, and a DIBL of 140 mV/V, indicating no obvious

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SCEs. However, the mobility of this fabricated FET is only 0.37 $cm^2/V{\cdot}s$ because of the substantial contact resistances, which play a major role in short-channel FETs. After excluding contact resistances, the mobility can theoretically be improved to 17.4 $cm^2/V{\cdot}s$.

Schematics of the fabrication of nanogaps are given in Figure 1a−d where first, a layer of ZEP-520A resist (ZEP) was spin-coated onto the substrate, upon which a layer of horizontally-aligned SWCNTs coated with a layer of poly(methyl methacrylate) (PMMA) was then transferred. The horizontally-aligned SWCNTs were grown by chemical vapor deposition (CVD) on a quartz substrate, and the SWCNT layer was transferred by a PMMA-assisted transfer method.[19]

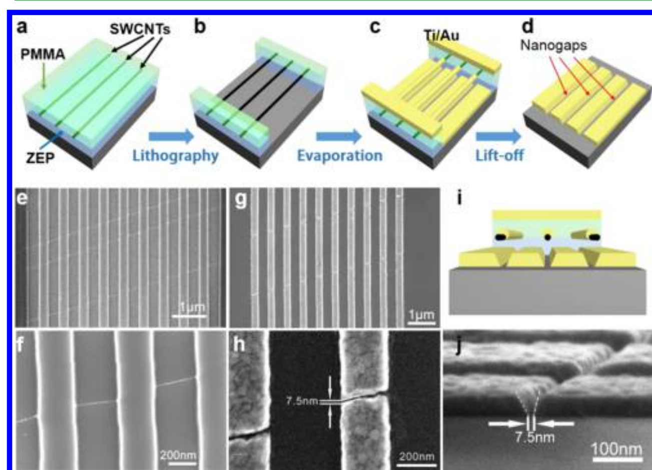

Figure 1. Fabrication process and SEM images of nanogaps. (a−d) Schematic diagrams of the nanogap fabrication process. (e,f) Top-view SEM images of SWCNTs suspended in trenches at two different magnifications. (g,h) Top-view SEM images of nanogaps in electrodes at two different magnifications. (i) Side-view schematic diagram of nanogaps and suspended SWCNTs. (j) Side-view SEM image of nanogaps.

Thus, a sandwich structure film consisting of ZEP/SWCNTs/PMMA was obtained on the substrate. In practice, the SWCNT direction could be controlled during transfer to roughly align with a certain edge of the substrate for the convenience of the next step. A set of parallel trenches roughly perpendicular to the SWCNTs were defined in the sandwich film by electron beam lithography (EBL). As a result, a portion of the SWCNT length was suspended on the substrate, whereas the rest was sandwiched between the ZEP and PMMA layers. Scanning electron microscope (SEM) images of the suspended SWCNTs are shown in Figure 1e,f. Using the suspended SWCNTs as a shadow mask in electron beam evaporation followed by lift-off, we obtained electrodes with gaps only several nanometers wide. Owing to the large-area uniform density of the horizontally-aligned SWCNT film, nanogaps were fabricated on a large scale with a high yield. Top-view SEM images of the electrodes with nanogaps are shown in Figure 1g. Typically, the nanogap width was around 7.5 nm, as shown in Figure 1h. In addition, metal layers were also deposited on the SWCNTs, and thus the SWCNT diameters gradually increased during the evaporation process. This induced a V-shaped cross-section of the nanogaps, as illustrated in Figure 1i. A side-view SEM image (Figure 1j) of the nanogaps clearly shows the V-shaped geometry, and the 7.5 nm width of the nanogap at the bottom (as measured) matches the top-view SEM measurement.

To study the stability and repeatability of the method herein, the process parameters that affect the widths of nanogaps were investigated. Considering that the diameters of the horizontally-aligned SWCNTs grown by CVD are quite uniform,[20,21] the nanogap widths (W) would only depend on the geometrical factors of the suspended SWCNT height (H), the suspended SWCNT length (L), and the thickness of the deposited metal (D) (shown in Figure 2a). Obviously, H is equivalent to the thickness of the underlying ZEP resist layer, and thus H can be adjusted by the spin coating speed. Furthermore, L is the width of the trench, which can be adjusted by the exposure width in the EBL process, and D

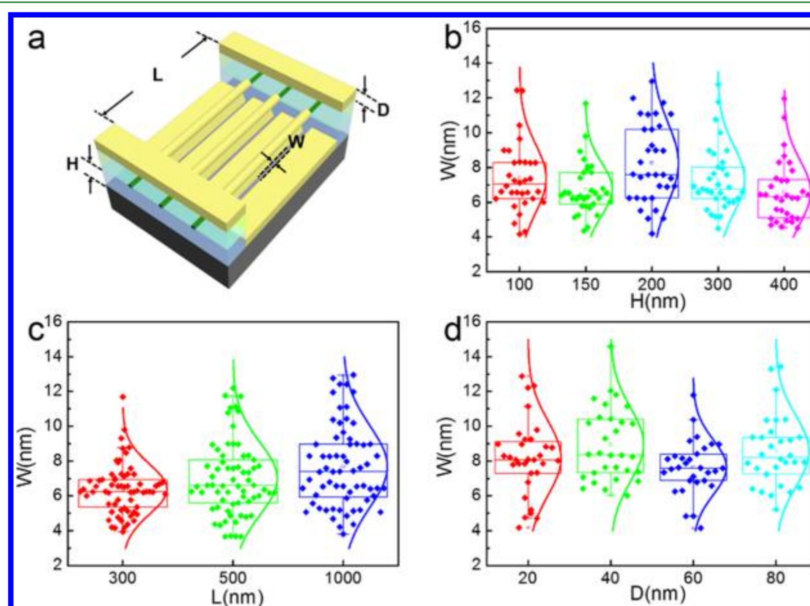

Figure 2. Stability of the nanogap width (W) for various process parameters. (a) Schematic diagram displaying the main process parameters. (b−d) Statistical distributions of the nanogap, W, for various values of suspended height (H) and length (L) of SWCNTs and metal thickness (D).

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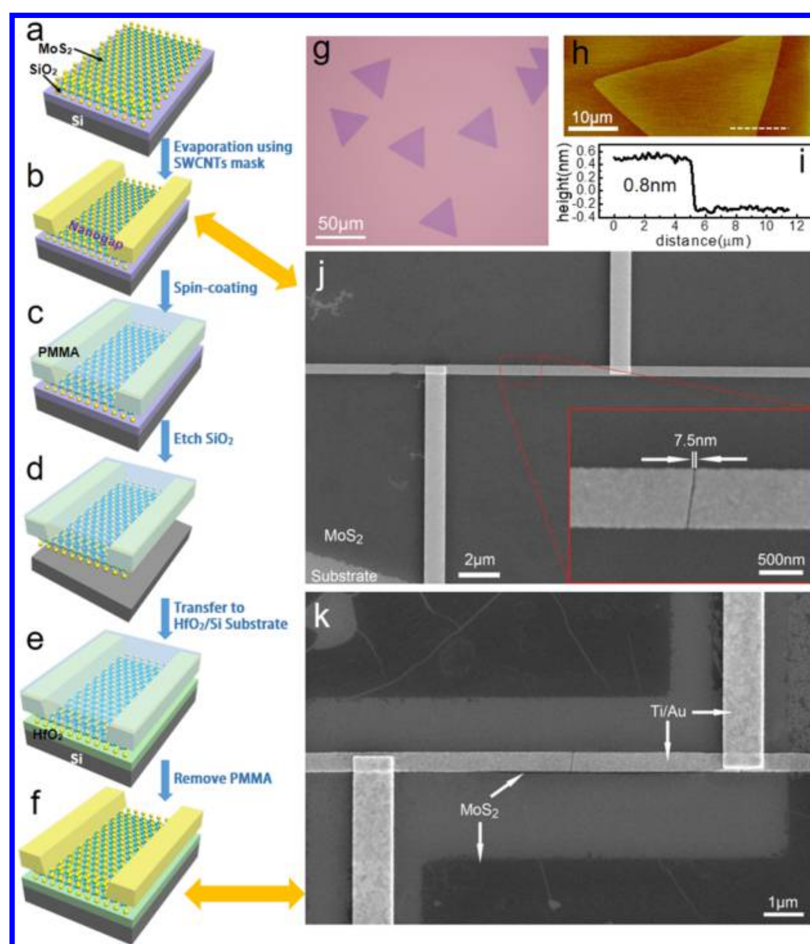

Figure 3. Fabrication process and SEM images of sub-10 nm monolayer MoS_2 FETs. (a−f) Schematics of the nanogap fabrication process. (g) Optical microscope image and (h) AFM image with height profile overlay; and (i) Raman spectra of the as-grown MoS_2. (j,k) Corresponding SEM images of (b,f), respectively, where the inset of (j) shows the details of a 7.5 nm channel length device.

directly depends on the evaporation time. The statistical distributions of W, as a function of H, L, and D are shown in Figure 2b−d, respectively. The average of the W value is around 7 nm for all process parameters, and it does not change significantly for both H varying in the range of 100−400 nm and D varying in the range of 20−80 nm. However, W exhibits a slight incremental change as L increases from 300 to 1000 nm, where this incremental change of W can be attributed to the intrinsic thermal vibration of the suspended SWCNTs.[22] The thermal vibration amplitude increases with the suspended SWCNT length and expands the effective SWCNT diameter, thus inducing the slight increase of W with L. The method herein also has some limitations in the process parameters, where the values of H, L, and D cannot exceed certain thresholds for optimal nanogap yield. With regard to the parameter D, for example; if D approaches the value of H, the suspended SWCNTs will be buried in the metal layer, causing a failure of the lift-off procedure. Nevertheless, our results suggest that the nanogap widths fabricated by this method are very stable in a wide process window.

On the basis of the method herein, sub-10 nm monolayer MoS_2 FETs were fabricated using the process shown in Figure 3a−f. The monolayer MoS_2 used herein was synthesized on a 285 nm thick SiO_2/Si substrate via CVD. Figure 3g,h give optical and atomic force microscope (AFM) images of the as-grown MoS_2, respectively. The height profile obtained along the white dashed line in Figure 3h and the Raman spectra in Figure 3i reveal that the MoS_2 thickness is 0.8 nm, which confirms that it is a monolayer. An SEM image of the monolayer MoS_2 FET with 7.5 nm channel length is presented in Figure 3j. To produce a strong suppression of SCEs, the channel length (L_{ch}) should be larger than the characteristic length,[23] $\lambda = [(\varepsilon_s t_s t_{ox})/\varepsilon_{ox}]^{1/2}$, where ε_s and ε_{ox} are the dielectric constants of the semiconductor and gate oxide layer dielectric, respectively; and t_s and t_{ox} are the thickness of the semiconductor and gate oxide layer, respectively. In the case of monolayer MoS_2 as the semiconductor ($\varepsilon_s = 3.3$, $t_s = 0.65$ nm) and 285 nm thick SiO_2 as the gate oxide layer ($\varepsilon_{ox} = 3.9$), the characteristic length, $\lambda = 12.52$ nm, which is excessively large compared to the channel length of 7.5 nm. To shorten the characteristic length, therefore, we transferred the entire device to a Si substrate with 10 nm thick HfO_2 as the dielectric layer, in which the HfO_2 layer was deposited via atomic layer deposition (ALD) at 90 °C. The dielectric constant of the HfO_2 layer was measured to be about 11.5 (Figure S2), and the capacitance of per unit area (C_i) is about 1.02 $\mu F/cm^2$. Therefore, the characteristic length was decreased to 1.37 nm, with which it is predicted that transistors will not exhibit SCEs.

The method used for transferring the entire device was almost the same as that used for transferring the horizontally-aligned SWCNTs to the ZEP resist layer. Direct transfer of the entire device avoided the accumulation of residue between MoS_2 and electrodes, thus, simultaneously reducing the contact resistances. To investigate the effect of the transfer

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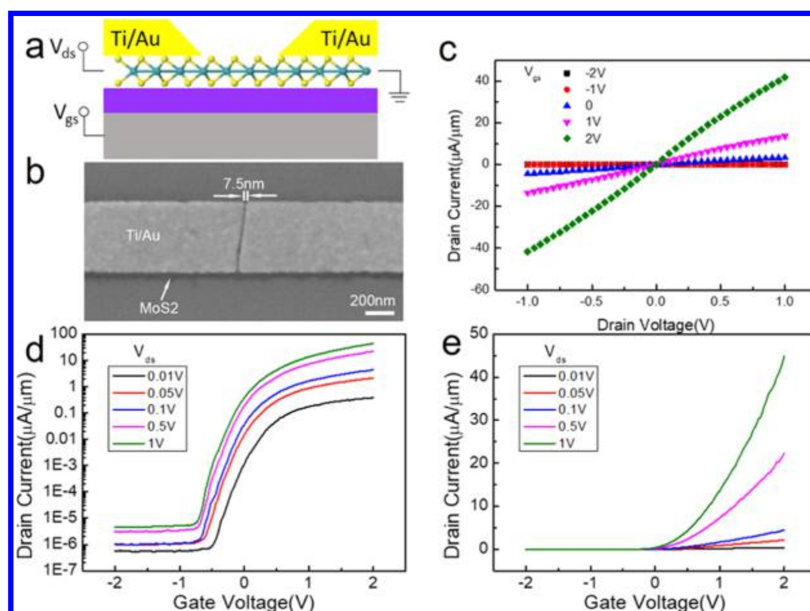

Figure 4. (a)Schematic and (b) SEM image of a 7.5 nm channel length monolayer MoS_2 FET. (c) Output and (d,e) transfer characteristics of the device showing strong suppression of SCEs and ohmic contact between the monolayer MoS_2 and metal electrodes.

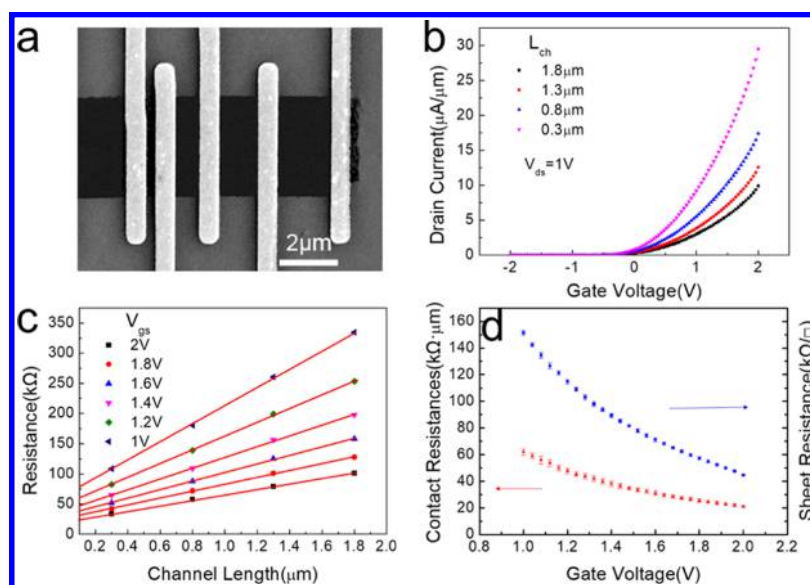

Figure 5. Contact resistances between monolayer MoS_2 and Ti/Au electrodes obtained from the TLM devices. (a) SEM image of monolayer MoS_2 FETs in the TLM geometry. (b) Transfer characteristics of MoS_2 FETs at various channel lengths. (c) Total resistance of MoS_2 FETs vs channel length at various gate voltages (V_{gs}), where solid lines are the linear fits. (d) Contact resistances ($2R_c$) (left axis) and sheet resistance (ρ) (right axis) extracted from linear fittings in (c) vs V_{gs}.

process on MoS_2, we characterized MoS_2 before and after transfer by Raman and photoluminescence (PL) spectra (Figure S3). The as-grown MoS_2 exhibited two Raman peaks at 381.1 and 404.1 cm^{-1}, whereas the transferred MoS_2 exhibited two Raman peaks at 385.0 and 404.1 cm^{-1}. This indicates that the as-grown MoS_2 is a monolayer according to a previous report,[24] and that strong interactions exist between the as-grown MoS_2 and the SiO_2 layer. Compared with the as-grown MoS_2, the PL intensity was quenched in the transferred MoS_2, which can be explained by the weakness of the interaction between MoS_2 and HfO_2 owing to the larger spacing after transfer and the lower Coulomb scattering of high-κ dielectrics. Therefore, compared with as-grown MoS_2 on SiO_2, the transfer process exhibited little damage to MoS_2 and weakened the interaction between MoS_2 and substrate, which is beneficial to high mobility. Subsequently, the channel width of the sub-10 nm MoS_2 FET was defined using EBL followed by O_2 plasma reactive ion etching (RIE). Figure 3k shows an SEM image of the MoS_2 device featuring a 7.5 nm channel length and a channel width (W_{ch}) of about 0.5 μm.

Considering that monolayer MoS_2 is very sensitive to illumination[25,26] and adsorption,[27,28] we tested the performance of the 7.5 nm channel length monolayer MoS_2 FET in the dark and in a vacuum (10^{-3} Pa) chamber. Figure 4a,b shows a schematic and a SEM image of the 7.5 nm channel length MoS_2 FET, respectively. Owing to the mismatch of EBL, a very narrow strip of MoS_2 remains at the electrode edges after RIE. The output characteristics of the device are given in Figure 4c,

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where the linearity of the output characteristics indicates an ohmic contact between MoS_2 and the Ti/Au electrodes. The transfer characteristics in logarithmic and linear scales are given in Figure 4d,e, respectively. The transfer curves indicate that the drain current ON/OFF ratio is between 10^6 and 10^7, and the ON-state current density is about 45 μA/μm at the gate voltage, V_{gs} = 2 V and the drain voltage, V_{ds} = 1 V. The subthreshold swing is estimated to be about 120 mV/V. The shift of the threshold voltage is about 140 mV when V_{ds} varies from 0.01−1 V, and thus the DIBL is about 140 mV/V.

However, the mobility estimated by the equation, $\mu = [dI_{ds}/dV_{gs}] \times [L_{ch}/(W_{ch}V_{ds}C_i)]$ is only 0.37 cm^2/V·s, which can be attributed to the substantial contact resistances in the device, which are especially present in ultrashort-channel transistors. To obtain the intrinsic mobility of this ultrashort-channel device, we need to extract the contact resistances ($2R_c$) using the transfer length method (TLM) and then exclude the value of $2R_c$ from the total resistance.

Figure 5a shows a SEM image of the TLM devices with stepped channel lengths of L_{ch} = 0.3, 0.8, 1.3, and 1.8 μm. In fact, the contact resistances between MoS_2 and metal will not change until the contact length (L_C) decreases to the transfer length (L_T, about 30 nm for MoS_2),[29] and therefore the contact resistances of the TLM devices should be the same as those in ultrashort-channel devices. Despite this, to guarantee that the contact resistances of the TLM devices were consistent with those of the ultrashort-channel devices, the TLM devices were fabricated using the same process as that for the ultrashort-channel devices, including transferring the devices to an HfO_2/Si substrate and defining the channel via RIE.

The electrical characteristics of the TLM devices were also measured in the dark and in a vacuum chamber, and the transfer curves for each channel length (L_{ch}) are given in Figure 5b. The loop sweep transfer curves of a long-channel (1.8 μm) and a short-channel (7.5 nm) MoS_2 FETs both show obvious hysteresis, indicating the precence of trap states in the channel and at the HfO_2/MoS_2 interface (Figure S4). It is simple to calculate the total resistance (R_{tot}) of each device at different V_{gs} values and put them into the $R_{tot}-L_{ch}$ plot, as shown in Figure 5c. The R_{tot} values have a good linearity with the L_{ch} values at each particular V_{gs}. For long-channel FETs, $R_{tot} = \rho L_{ch} + 2R_c$, and therefore $2R_c$ equals the intercept and ρ equals the slope of the fitting line. The values of $2R_c$ and ρ are thus extracted from the linear fits and are given in Figure 5d. Because no obvious SCEs are present, the voltage drop on the channel is $V_{ds} \times (R_{tot} - 2R_c)/R_{tot}$. Hence, the intrinsic mobility, μ, can be deduced using the equation, $\mu = [dI_{ds}/dV_{gs}] \times [L_{ch}/(W_{ch}V_{ds}C_i)] \times [R_{tot}/(R_{tot} - 2R_c)]$, and herein was calculated to be about 17.4 cm^2/V·s (Figure S5), which is consistent with previous reports(Table S1).[13,14,30] Futhermore, R_c as given by the Y-function is about 16.8 kΩ·μm (Figure S6), which is close to the TLM results of about 10.5 kΩ·μm. It is therefore essential to reduce the contact resistances of the MoS_2 FETs for application in ultrashort-channel length transistors.

CONCLUSIONS

In conclusion, we developed herein a method to fabricate sub-10 nm gaps in electrodes using horizontally-aligned SWCNTs as an evaporation mask. The nanogap widths exhibited strong stability to various process parameters, indicating that this method is highly suitable for large-scale fabrication. Monolayer MoS_2 FETs with sub-10 nm channel length were fabricated by the method and exhibited superior suppression of SCEs. We also found that the contact resistances were prominent in these ultrashort-channel devices. This work provides a universal and stable method for the large-scale fabrication of ultrashort-channel 2D materials transistors.

METHODS

Sample Preparation and Characterization. Both the horizontally-aligned SWCNT film and monolayer MoS_2 were synthesized by CVD. The horizontally-aligned SWCNTs were grown on a stable temperature-cut quartz substrate, whereas the monolayer MoS_2 samples were grown on a 285 nm thick SiO_2/Si substrate. Details of the MoS_2 CVD process are given in the Supporting Information. The parallel alignment of the CNTs is naturally formed during the growth process, which can be attributed to the high speed of CH_4 flow. The direction of SWCNTs can be controlled during the transfer process to make them roughly parallel to a certain direction of the substrate. PMMA is widely used in the transfer process for its good mechanics, thus, we use PMMA coating of the nanotubes for transferring. All SEM images were taken with a Nova NanoSEM 450 scanning electronic microscope. All AFM images were taken with a Veeco Dimension V AFM. All Raman and PL spectra were taken with a HORIBA LabRAM HR Raman spectrometer.

Nanogap Fabrication. The PMMA 1950 A4 (MicroChem company) layer was spin-coated at 3600 rpm for a thickness of about 200 nm, and the ZEP520A (ZEON Chemicals) layer was spin-coated at 5500 rpm for a thickness of about 300 nm, whereupon the resist layers were prebaked on a hotplate at 180 °C for 90 s. EBL was performed using a JEOL JBX-6300FS system operated at 100 kV, a beam current of 400 pA, a beam diameter of 3 nm, a writing field of 62.5 μm, and an exposure dose of 1000 $\mu C/cm^2$. The resist development was carried out in amyl acetate for 90 s at room temperature followed by rinsing in isopropyl alcohol. After metal deposition by electron beam evaporation, the two resist layers were removed in methyl ethyl ketone.

Transistor Fabrication and Measurement. The contact electrodes of the sub-10 nm channel length MoS_2 transistors were Ti (5 nm)/Au (50 nm) electrodes. The transistors were initially fabricated on a 285 nm thick SiO_2/Si substrate and subsequently transferred to a 10 nm thick HfO_2/Si substrate, where the HfO_2 film was deposited by ALD at 90 °C. The electrical measurements were carried out on a probe station (TTP, Lakeshore, USA) equipped with a vacuum pump and a semiconductor characterization system (4156C, Agilent, USA).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b21437.

CVD growth of monolayer MoS_2, measurement of HfO_2 dielectric constant, Raman and PL spectra of as-grown and transferred MoS_2, hysteresis of long-channel and short-channel MoS_2 FETs, transfer characteristics after excluding contact resistances, comparison of the contact resistance and sheet resistance of MoS_2 FETs, and contact resistance extracted by Y-function (PDF)

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Notes

The authors declare no competing financial interest.

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